REMARKS

Dear Sir:

This is a Response to the Office Action in the above referenced application mailed on May 30, 2006, and for which a 2-month extension is hereby requested. The Office Action rejected pending claims 3-11 and 15-25 under 35 U.S.C. 103(a) with European Patent Application Publication number 0 292 248 of Steiner et al. as the primary reference. It is respectfully submitted that these rejections are not well founded.

Claim 3 is the first independent claim:

> An add-on card for detachably coupling to a processing system comprising:
> an interface for communicating with said processing system while said add-on card is coupled with said processing system;
> a program storage memory storing at least one operating sequence;
> *a **mass storage memory** including a portion for storing **user data*** and a program memory portion storing at least one additional operating sequence;
> a processing unit coupled to said interface, said program storage memory, and said mass storage memory, whereby the processing unit can operate on user data transferred between the mass storage memory and the processing system through the interface according to said at least one additional operating sequence;
> a card bus to which the processing unit, the interface and the program storage memory are connected; and
> *a mass storage interface* by which the mass storage memory is connected to the card bus, *wherein the mass storage interface is a **non-linear** interface.*

The emphasis has been added. The Office Action identifies the "add-on card" with "CARD" 3 in Steiner's Figure 1, identifies the "mass storage memory including a portion for storing user data" with Steiner's "Data Storage" 9, and just generally refers to Steiner's Figure 1 for the "mass storage interface". The Office Action admits that Steiner "does not explicitly disclose the mass storage interface is a non-linear interface", and then cites Robinson (US patent number 5,544,356 to Steiner et al.) to provide this missing element. These identifications and the rejections based upon them are respectfully submitted to be in error for a number of reasons.

The device of Steiner is "an electronic token of the 'smart card' type", as described there in the Abstract and elaborated in the first few paragraphs of its disclosure. As befits their function as electronic tokens, such smart card devices are of fairly limited ability and have relatively modest memory capacities. As shown in Steiner's Figure 2, the total amount of memory available for Application program and data memory *combined* is only 7k Bytes, since such devices only execute fairly simple applications and do not use much memory for data storage. As noted at column 3, lines 38-44, the memory has "a partition between the applications program area 8 and remainder of the

read/write memory region to establish a data storage area 9, in which *data relevant to the intended use of the card* can be stored and altered as desired": as the added emphasis notes, the data portion of the memory is for data relevant to what card is intended to be used for. This is typical of smart cards, and consistent with the description given in Steiner, where the data is system data maintained by the smart card-host system that relates to the transactions conducted with the smart card in its function as an electronic token. There is no suggestion of this data memory being used for general data of the user's choosing, but only for "data relevant to the intended use of the card". Also, although the Office Action states that Steiner's Figure 1 includes a "mass storage interface" for the memory, Figure 1 only shows that the memory (7, 8, and 9) are connected directly to the microprocessor 4. As is clear from Steiner's Figure 2 and its description, although shown as separate boxes 7, 8, and 9 in Figure 1, the operating system, applications program and data memory are all part of the same memory; and as the microprocessor needs to access any application programs or operating system linearly in order for it to be executed, even if there were such an interface it would be a linear interface. To introduce a *non-linear* interface, as suggested in the Office Action would first require the transferal of these elements to another memory, which Steiner neither teaches nor suggests, that is linearly accessible, a process that Steiner neither teaches nor suggests. Consequently, it believed that such an introduction of a non-linear interface is not only being improperly based upon hindsight gained from the present application but is also contrary to the teachings of the primary reference of Steiner.

More explicitly, claim 1 includes "a mass storage memory". As shown in Steiner's Figure 2, the total amount of writable memory (corresponding to both of blocks 8 and 9 in Figure 1) is 7 kBytes. It is respectfully submitted that this is not mass storage memory: As noted in the previous Response, "mass storage memory" is a term that would be understood in the art. For example, reference is made to US Patent Application Publication number US 2001/0052038 of Fallon et al., which is being submitted with the present Response as part of an Information Disclosure Statement. The Fallon patent application, which was filed a few months before the present application, includes a "Description of the Related Art" that can be taken as indication of what would have been understood in the art at the time the present application was filed. Several Wikipedia articles are also being submitted: Although these are of more recent origin, they give an indication of the use of "mass storage" in this context and make clear that the discussion in the Fallon application is

consistent with current usage rather than some aberrant usage. Although Steiner notes that the memory capacity may be varied, but there is still no suggestion of what would be understood "mass storage" as the term would have been understood in the art.

Claim 1 further states that the mass storage memory is "a mass storage memory *including a portion for storing user data*", where the emphasis is added. As noted above, Steiner does not disclose that "Data Storage" 9 (in Figure 9, labeled as "Data memory" in Figure 2) is for storing user data; rather, it is for storing system data used by the host-card system for the various token type functions for which smart cards are employed. As noted above, Steiner uses this memory for "data relevant to the intended use of the card".

The final element of claim 1 is "a mass storage interface by which the mass storage memory is connected to the card bus, wherein the mass storage interface is a non-linear interface." Although Steiner's Figure 1 shows three separate blocks 7, 8, and 9, as is clear from Figure 2 and from the description given in column 3 (particularly beginning at the end of the first full paragraph), these are areas are all part of the same physical memory. This is believed to be particularly clear with respect to "Application program" portion and the "Data memory" portion as the partition between these is movable, with the "application program" part taking that of the 7K Bytes that it needs, with the rest left over for "Data memory". The Office refers general to Steiner's Figure 1 for a memory interface, but is respectfully submitted that each of blocks 7, 8, and 9 are shown as directly connected to microprocessor 4 without any explicitly interface indicated. The Office Action states that it "would have been obvious to one of ordinary skill in the art at the time the invention was made" to incorporate a non-linear interface (with the Robinson reference cited for such an interface); however, it is respectfully submitted that not only would this *not* be obvious, but would be *contrary* to what Steiner presents. In Steiner, both "Application program" and "Data memory" are part of the same memory. For the microprocessor 4 to implement an application program, the code of the application will need to be linearly accessible. Consequently, an access of the memory of Steiner, and any interface used for this purpose, would be linear. If instead such an interface were non-linear, its contents would need to be accessed non-linearly and stored in another memory, from which it could be accessed linearly in order to execute the application. Steiner has no discussion of such an additional memory so that memory 8/9 is thus needed to be linearly accessible. Consequently, it is again respectfully submitted that the Office Action is improperly interpreting the references based

upon hindsight gained from the present application and combining them in ways that are contrary to the teachings of the primary reference. (Further, concerning the remarks made in the Office Action, it is again noted that "flash" refers to the erase structure of a memory, rather than how it is necessarily accessed.)

The Office Action rejected the other independent claim, claim 15, on the same basis as claim 3; as claim 15 includes the particular elements discussed above with respect to claim 3, it is similarly believed allowable for at least the reasons given above for claim 3. Many of dependent claims are also believed further allowable for the various additional limitations that they recite, but as their underlying independent claims are believed allowable for the multiple reasons given above, these will not be presented at this time.

For the reasons given above, it is therefore respectfully submitted that the rejection of claims 3-11 and 15-25 is not well founded and should be withdrawn. Reconsideration of these claims and an early indication of the allowance of the present application are earnestly solicited.

Respectfully submitted,

Gerald P. Parsons
Reg. No. 24,486

10/25/06
Date

PARSONS HSUE & DE RUNTZ LLP
595 Market Street, Suite 1900
San Francisco, CA 94105
(415) 318-1160 (main)
(415) 318-1163 (direct)
(415) 693-0194 (fax)